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# Data Path

The detector data path through the FPGA, shown in blue, begins with the digitized ASIC data input from the ADC. Each FEB will process a serial data stream from 32 APD channels. The processing of each channel will time share the same FPGA resources, but remain functionally independent. The data will first be deserialized and time-stamped then sent to the Data Processing block where it is sparsified and buffered. The buffered data is formed into packets in the DCM interface and transmitted to the DCM.

## ADC Deserialization

## Timing

The FEB uses an internal time counter to timestamp the APD data. The time is synchronized across different FEBs using the Sync signal on the FEB-DCM link. When the FEB receives the Sync signal it will set the current time to a preset parameter. The current time can be started and stopped using the corresponding FEB commands.

## Data Sparsification and Triggering

The FEB data sparsification uses a magnitude over-threshold scheme where a FIR filtered version of the channel’s data is compared to a preset threshold. If the magnitude exceeds the threshold, an event will be triggered and the corresponding data from the triggered channel will be buffered until it can be sent to the DCM. The trigger will look for a maximum value over the threshold during a single event rather than the first value over threshold. The FIR filter coefficients used are [1 0 0 -1]. The characteristics of this filter will be dependent on FEB version as the sampling rates are different. In the case of the FEB4.X, the filter will be the difference of samples that are separated by 1.5us. In the case of FEB5.X, the filter will be the difference of samples that are separated by 375ns. The triggering threshold can be uniquely set for each channel.

When an event is triggered, the FEB will collect a number of continuous samples, before and after, the sample that triggered the event. The number of samples collected before and the number of samples collected after is a settable parameter. This format is referred to as multipoint readout.

The FEB will include a diagnostics mode where the sparsification trigger can be turned off, referred to as “oscilloscope mode”. In this mode, the FEB will operate similar to a digital storage oscilloscope. The digitized APD data from the enabled channels will be buffered in one continuous time slice. Since the buffer memory is fixed and shared between all channels, the length of the time slice is determined by the number of channels that are enabled. Oscilloscope mode is used in conjunction with the FEB's pulse generator functionality. When the FEB is enabled and ready to take data, the data buffer must be 'triggered' using the internal pulser signal. If the Event buffer becomes full, it will signal the FEB to stop taking data and put itself in idle mode. The number of contiguous samples returned is determined by the FEB to DCM throughput, data buffer depth, and number of channels that are enabled. The FEB can be set to limit the number of samples that are returned.

## DCM Interface

The DCM interface will coordinate the data that is sent between the DCM and FEB. The data is sent using a 8b10b protocol. The command signal is used to send register read and write requests from the DCM to the FEB. The data signal is used to transmit data from FEB including triggered APD data, timing data, status data and register read data. Information on this protocol can be found in NOVA-doc-814-v6,” Link Interface Specification for the Nova Front End Board to Data Concentrator Module Connection”.

# Control

The control block will coordinate the operation of the FEB and serve as an interface to components on the FEB that are external to the FPGA. It utilizes a combination of commands and registers to control the operation of the FEB. Registers are used to set FEB parameters and commands are used to change FEB modes of operation or initiate an event.

## ASIC Programming

The ASIC contains several configuration registers. The Control block will provide an interface to the ASIC configuration registers and allows it to be configured using the standard DCM interface register read and write commands. The FEB has a register for each settable ASIC parameter. Once all of the ASIC registers have been set, the FEB Set ASIC command will transfer the configuration to the ASIC. This will also transfer the previous ASIC configuration back into the corresponding FEB registers. This ASIC configuration loop provides a verification that the configuration is properly being received by the ASIC.

## SPI Interface

There are several components on the FEB that use the SPI bus communication protocol. The Control block provides a SPI bus interface to these components using the standard DCM interface register read and write commands. These components include a temperature sensor, 128 byte EEPROM used to store the board serial number, and a ADC and DAC used to interface with the TECC and high-voltage regulator.

## TECC Control

The TECC is controlled by providing an analog “Setpoint” along with Enable signal. The TECC is monitored by reading the values of two analog signals, “DriveMonitor” and “TempMonitor”. The ADC and DAC used in this interface are controlled by the FEB using the SPI interface. The FEB will provide access to the TECC through the DCM interface

The FEB will automatically monitor the temperature and drive signals reported from the TECC and look for potential problems in the APD cooling system that could physically damage the detector. The FEB will automatically disable the TECC and flag an error condition if the temperature monitor is too high or the drive monitor is too high for a configurable amount of time. The threshold levels that generate errors are fixed values and the time threshold is programmable and measured in minutes.

## High Voltage

The ADC used in the high voltage regulator is controlled by the FEB using the SPI interface. The FEB provides access to the regulator through the DCM interface.

## Pulse Generator

The FEB contains a configurable pulse generator, only used in testing and debugging, that provides a way to synchronize the digitization of APD data with external stimulus such as ASIC charge injection. The pulse generator signal can be sent to any of three locations, the data readout trigger, the ASIC charge injection, and a FEB external connector that can trigger external instruments. The pulser signal that is sent to the read out trigger is advanced by a fixed amount to allow samples prior to an external event to be also included in the data. This synchronization is required to catch the data that corresponds with an external stimulus. The Pulser Enable bits determine what part of the FEB will see the pulse. A common test preformed is to start the FEB in oscilloscope mode and begin to record the digitized data. The external pulse is then used to trigger a calibrated injection of charge. The digitized data is then read out and analyzed. The pulser can also be set to periodically inject charge into the ASIC and generate a constant stream of events that are process as they would be if received from an APD.

# Clock Generator

The Clock Generator contains a PLL to generate all of the clocks required by the FEB using a 32 MHz reference clock provide on the DCM Interface link. The logic primarily uses the 64 MHz and 128 MHz clock. The FEB also uses 4MHz, 16MHz, and 32MHz timing synchronization.

# Soft Power-up

FEB V5.x consumes 1.1 amps of current on the Low Voltage supply where 50% of this current is required by the 2 ADCs on the board. When 64 FEBs, which are attached to one Power Distribution Box, are synchronously programmed with firmware or un-programmed with the sync signal, they produce a 50 amp current step. This step, in conjunction with the power supply sense cable feedback-loop, produce a voltage ringing on the power supply which has amplitude which falls outside the preset limits. To eliminate this problem, each FEB will delay the powering of the ADCs by a different amount; distributing a single large step into smaller steps. Once programmed with firmware, the FEB will read its serial number which is stored in external memory. The last 2 digits of this serial number will dinnertime the amount to delay the power-up of the ADC. The ADC power-up will happen automatically when the FEB is programmed with firmware. If the FEB is going to be un-programmed, as happens when a currently programmed FEB is about to be re-programmed, a command will need to instruct the FEB to power-down the ADCs in the same manner. The length of the ramp will range from 0 to 10ms The power state of the ADC will be reported in the status register. This feature is only functional in the Version 5. Any related commands sent to version 4 will safely be ignored.